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ECe 3200-01 Lab 6

Common Collector Amplifier

**Objective:**

The objective of this lab is to measure the biasing stability of an NPN & PNP transistor circuits and validate the results by calculation and simulation. As a result, students will have a foundation for the design of small signal amplifiers.

**Prelab:**

1. Design a common collector amplifier using a 2N3904, NPN transistor to meet the DC specification ICq = 7.5 mA and VCEq = 6 V. Use IR1 = 10x Ibq and IR2 = 9xIbq criterion to design the voltage divider network (see diagram ) . Assume the current gain, β , is equal to β = 150 . The supply voltage is **VCC = 15 V** . **Use standard resistor values.**
2. Use the small signal hybrid-π model to analyze and predict the mid-band frequency. a) the voltage gain AV = vo / vi , b) the input resistance Ri = vi / Iin and c) the small signal output resistance Ro external to the RL =1 kΩ while Rg = 4.7 kΩ is in place.
3. Determine the value of the capacitor CC2 so that the **cutoff frequency** due to the time constant CC2 RL will be approximately set at 600 Hz. Then estimate CC1 so that its reactance, XCc1, will be negligible at 600 Hz (Hint : XCc1 << Rg + Ri at 600 Hz).
4. Estimate the maximum peak-to-peak (MPP) unclipped voltage swing available at the output.

MPP < 2 x smaller of { (VCEq – 0.7) or ICq( RE|| RL)}

P = 5.3 Vp N = 4.1 Vp …Est. From Calc

Text, letter

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**Parameter Values**:

RE = 1.2 kΩ , R1 = 10 kΩ , R2 = 22 kΩ, CC2 = 0.27 μF , CC1 = 0.22 μF

**Results and Measurements:**

Build the circuit with your calculated values and make the following DC and AC measurements.

1. DC Measurements:

Diagram, schematic

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With the signal generator OFF (or amplitude set at its minimum) measure,

VCEq = 5.64 V , IC ≈ IE = 7.8 mA , VB = 9.96 V

Data is from the following measurements: VC = 15 V, VE = 9.36 V, VB = 9.96 V, IC ≈ IE= = 9.36 V/ 1.2k = 7.8 mA

Compare the measured values versus the design specification and calculate the % of discrepancy.

% VCEq = …6.00… % IC = …4.00…% , VB = …2.68… %

1. AC Measurements:

Set the signal generator to Vg = 2 Vpp at about 10 to 12 kHz . At this frequency the reactance of the DC coupling/decoupling capacitors will have a minimal effect over the measurements.

Measure the following AC performance parameters:

Theoretical Values:

vi = 1.21 Vpp , vo = 1.19. Vpp with RL = 1 kΩ .

Measured Values:

vi = 1.12 mVpp , vo = 1.035 mVpp with RL = 1 kΩ .

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**Calculate Ri and Av from your measurements**,

Theoretical Values:

Ri = Rg vi /( Vg – vi ) = 4.7 k x1.21 / ( 2 – 1.21) = 7.2 k

and AV = vo /vi = 1.19 Vpp / 1.21 Vpp= 0.98

Measured Values:

Ri = Rg vi /( Vg – vi ) = 4.7 k x 1.123 m/ ( 2 – 1.123m) = 6.02 k

and AV = vo /vi = 1.035 mVpp / 1.123 mVpp= 0.922

Compare Ri and AV versus the values obtained from the analysis in the pre lab and determine the % of discrepancy,

% Ri = 16.3889%, % AV = 5.91837%

**Checking Cutoff Frequency**

Now reduce the **frequency** of the signal generator towards the lower end until the value of output , recorded before at around 10 kHz , drops to 0.707vo . Record the signal generator frequency , fC , this is the measured lower cutoff frequency,

fC = 560 Hz. (Theoretical Value)

fC = 620 Hz. (Measured Value)

What is the discrepancy between the measured cutoff frequency and the designated

600 Hz?

% fC = 10.7143%

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**Measuring the output resistance Ro external to RL,**

In order to measure Ro remove RL = 1 kΩ load resistor (i.e. set RL = ∞) and increase the generator frequency to 100 kHz. This action will ensure that the AC voltage drop across the capacitor C2 still can be considered negligible as the load resistor is about to be reduced by 10-fold.

Now measure the output **open circuit** signal (i.e. without RL),

vo ( without RL ) = 1.21 Vpp

Again measure the output , vo (with RL ) with a new value of RL = 100 Ω . **Such test resistors must be chosen to be small enough to make a measurable drop at the output but yet not too small to cause a severe signal distortion .**

vo ( with RL) = 0.930 Vpp

Now calculate Ro from,

Ro = RL [ vo(without RL ) - vo ( with RL) ] / vo(with RL) = 30. Ω .

Compare the value verses the calculated one in prelab and determine the % of discrepancy,

% Ro = 40.1869%

**Measuring MPP output voltage swing (est.).**

Restore the load resistor, RL , to RL = 1 kΩ and the signal generator frequency back to 10 to 12 kHz . Increase the signal generator amplitude gradually and observe the output until the on set of distortion. Record the peak-to-peak output and compare versus the estimated one in the part 4 of the prelab.

Is there an agreement?

MPP(measured) = 4.25 Vpp

MPP(calculated) = 4.05 Vpp

MPP(% error) = 4.93827%

When comparing the measurements found in the procedure, and the calculated values, we can see that there is small % error between the calculated and measured MPP values. This error may be prevalent, due to the beta value used for the 2N3904. Regardless of the small percent error, I was still able to understand how to calculate the maximum peak-to-peak unclipped voltage swing at the output.

**Conclusion:**

This lab was conducted to examine the effects of a Common Collector (CC) amplifier given both DC and AC input voltage sources. As a result of this lab, I was able to better understand how to construct a simple CC amplifier to meet a specific bias condition and a specific voltage gain, Av. By utilizing the 2N3904 NPN transistor and pSpice, I was able to determine the AC and DC current gains as well as the output and input resistor value at the Q-point. Although I was not able perform the lab physically, I was still able to visualize and understand the circuit with the help of pSpice, and the zoom meeting provided.